

**IN THE CLAIMS:**

1. (currently amended)      An apparatus for correcting programmatic time-gap defects in a computer system configured to communicate with devices of both synchronous and asynchronous types, the apparatus comprising:

a processor configured to process data communicated with devices of both synchronous and asynchronous types; and

a controller comprising a buffer having a capacity of bytes and configured to temporarily store the data exchanged, the controller configured to control an exchange of data between the devices and to generate at least one content limiting interrupt corresponding to a near capacity condition of the buffer, [the controller including a buffer, having a capacity of bytes and configured to temporarily store the data exchanged], and

a memory device operably connected to the processor to store data structures comprising executables, the executables comprising:

a driver configured to control operation of the controller, and

an error avoidance module, the error avoidance module configured to be invoked by the driver upon generation of the at least one content limiting interrupt to monitor the transfer of bytes with respect to the buffer and to compare the capacity to a count of bytes transferred with respect to the buffer, and to force an error based on the comparison.

2.(previously presented)      The apparatus of claim 1, wherein the error condition is forced if the value of the count corresponds to transfers of bytes causing exhaustion of buffer capacity.

3. (canceled)

4.(currently amended)      The apparatus of claim 1, wherein the driver further comprises an initialization module configured to enable executable data structures comprising the error avoidance module.

5.(previously presented)      The apparatus of claim 4, wherein the initialization module is further configured to enable the content limiting interrupt configured to occur when the content of the buffer approaches a capacity limit.

6.(canceled)

7.(canceled)

8. (canceled)

9. (previously presented)      The apparatus of claim 5, wherein the content limiting interrupt is configured to trigger the execution of the error avoidance module.

10.(previously presented)      The apparatus of claim 9, wherein the error avoidance module is configured to detect one of a read and a write operation.

11. (previously presented)      The apparatus of claim 10, wherein the error avoidance module is configured to detect both a read and a write operation.

12.(previously presented)      The apparatus of claim 11, wherein the buffer is selected from the group consisting of a register, a FIFO, and a content-addressable memory.

13.(currently amended)      A method for correcting programmatic time-gap defects in a computer system configured to communicate with devices of both synchronous and asynchronous types, the method comprising:

transferring bytes of data between a device and a buffer having a capacity;

providing a count of the bytes;

comparing the count to the capacity; and

forcing an error condition corresponding to an unsuccessful transfer based on the count.

14.(previously presented)      The method of claim 13, wherein the error condition is forced if the value of the count is at least as large as the capacity.

15.(currently amended)      A method for correcting programmatic time-gap defects in a computer system configured to communicate with devices of both synchronous and asynchronous types, the method comprising:

transferring bytes of data between a device and a buffer having a capacity;

providing a count of the bytes;

comparing the count to the capacity; and

forcing an error condition corresponding to an unsuccessful transfer of at least one of the bytes after transferring the bytes based on the count if the value of the count is at least as large as the capacity of the buffer added to a value corresponding to bytes that have been transferred both into and out of the buffer during a transfer operation.

16.(previously presented)      The method of claim 13, further comprising dynamically creating[enabling] a content limiting interrupt configured to occur when the content of the buffer approaches a capacity limit.

17.(previously presented)      The method of claim 16, wherein the capacity limit is a plurality of limits.

18.(previously presented)      The method of claim 16, wherein the capacity limit is selected from the group consisting of a high and a low limit.

19.(previously presented)      The method of claim 16, wherein the capacity limit is both high and low limits.

20.(previously presented) The method of claim 16, wherein the content limiting interrupt is configured to trigger the error avoidance module to initialize the count.

21.(previously presented) The method of claim 20, wherein the buffer is selected from the group consisting of a register, a FIFO, and a content addressable memory.

22.(currently amended)      An article including a computer readable medium configured to correct programmatic time-gap defects in a computer system having synchronous and asynchronous devices interconnected to one another, the apparatus comprising:

a controller driver comprising executable and operational data structures configured to control operation of a controller in the computer system;

an error avoidance module configured to count the number of bytes transferred with respect to a buffer used by the controller, during an exchange of data, and to force an error condition corresponding to a failed transfer based on the count.

23.(currently amended)      The apparatus of claim 22, wherein the controller driver further comprises an initialization module configured to modify executable data structures of the controller driver to enable the error avoidance module.

24.(currently amended)      An apparatus for correcting programmatic time-gap defects,  
the apparatus comprising:

a processor configured to communicate with devices of both synchronous and asynchronous types; and

a controller for controlling an exchange of data between the devices, the controller including a controller memory storing executable data structures for programmatically controlling the controller and a buffer, having a byte capacity; and

a memory device configured to store executables comprising:

a driver configured to control the controller and invoke an error avoidance module, the error avoidance module configured to compare the byte capacity to a count of bytes transferred with respect to the buffer, and to force an error condition based on the count, and

an initialization module configured to modify the executable data structures of the controller memory to generate an interrupt, the driver configured to invoke the error avoidance module upon generation of the interrupt.

25.(new) An apparatus for correcting programmatic time-gap defects in a computer system configured to communicate with devices of both synchronous and asynchronous types, the apparatus comprising:

a processor configured to process data communicated with devices of both synchronous and asynchronous types; and

a controller comprising a buffer configured to temporarily store the data exchanged and having a write capacity and a read capacity, the controller configured to control an exchange of data between the devices and to generate at least one FIFO interrupt corresponding to at least one of a nearly full condition of the buffer and a nearly empty condition of the buffer, and

a memory device operably connected to the processor to store data structures comprising executables, the executables comprising:

a driver configured to control operation of the controller, and

an error avoidance module, the error avoidance module configured to be invoked by the driver upon generation of a FIFO interrupt to monitor the transfer of bytes with respect to the buffer and to compare at least one of the read capacity to a count of bytes read from the buffer and the write capacity to a count of bytes written to the buffer, and to force an error condition based on the comparison.

26.(new) The apparatus of claim 25, wherein the error condition forced corresponds to an unsuccessful read or write operation.

27.(new) The apparatus of claim 26, wherein the memory further comprises an initialization module configured to enable the FIFO interrupt.